What is claimed is:

1. A method for fabricating a transistor in a semiconductor device, comprising:

forming an isolation region in a semiconductor substrate and sequentially depositing a pad oxide layer, a pad nitride layer and a first oxide layer on the substrate and the isolation region ;

pattering the first oxide layer and pad nitride layer to form a gate electrode;

depositing a doped poly silicon layer;

forming a doped polysilicon sidewall on the pad nitride layer and the first oxide layer;

etching the pad oxide layer;

sequentially depositing and planarizing a gate isolation layer, a gate nitride layer and a metal layer on the substrate to form the gate electrode; and

forming a source, a drain, a gate plug, a source plug and a drain plug, respectively.

2. The method of claim 1, wherein the isolation region is shallow trench isolation(STI).

3. The method of claim 1, wherein a thickness of the pad oxide layer is not less than 50 angstrom.

4. The method of claim 1, wherein a local channel ion implantation is performed only in case a source and a drain region is salicidated or a lightly doped drain (LDD) implantation is performed before depositing the gate isolation layer.

5. The method of claim 1, wherein the doped poly silicon sidewall is used to serve as the LDD implantation.

6. The method of claim 1, wherein the gate nitride layer is made of at least one of TiN and TaN.

7. The method of claim 1, wherein the metal layer is made of tungsten (W).

8. The method of claim 2, wherein the thickness of the pad oxide layer under the doped poly silicon sidewall is controlled to be used to serve as the LDD implantation.